Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-9. (Canceled).

10. (Previously Presented) A high-voltage MOS transistor comprising:

a substrate;

a gate structure overlying the substrate, the gate structure having a first side and a second side opposite to the first side;

a first doping region with a first dosage formed in the substrate on the first side of the gate structure and partially covered by the gate structure;

a second doping region with a second dosage formed within the first doping region adjacent to the edge on the first side of the gate structure to serve as a drain region and a third doping region with the second dosage formed in the substrate adjacent to the edge of the second side of the gate structure to serve as a source region; and

a channel region formed in the substrate between the first and third doping regions by turning on the high-voltage MOS transistor to pass current between the source and drain regions, where a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region,

wherein the first dosage is about 7.0 to 9.0E12 ions/cm^2.

11. (Original) The device as claimed in claim 10, wherein the second dosage is about 2.0 to 4.0E15 ions/cm^2.

12-23. (Canceled).

24. (Currently Amended) A high-voltage MOS transistor comprising:

a first drain region with a first dosage formed in a substrate, wherein the first drain region extends horizontally from a first point proximate to an upper surface of the substrate to a second point proximate to the upper surface;

a first source region with the first dosage formed in [[a]] the substrate, wherein the first source region extends horizontally from a third point proximate to an upper surface of the substrate to a fourth point proximate to the upper surface;

a gate structure overlying the substrate, interposed between the first drain region and the first source region, covering a portion of the first drain region extending from the first point to a fifth point of the first drain region located between the first and second points, and covering a portion of the first source region extending from the third point to a sixth point of the first source region located between the third and fourth points;

a first spacer in contact with the gate structure and covering a portion of the first drain region from the fifth point to a seventh point of the first drain region located between the fifth and second points;

a second spacer in contact with the gate structure and covering a portion of the first source region from the sixth point to an eighth point of the first source region located between the sixth and fourth points;

a second drain region with a second dosage formed within the first drain region, wherein the second drain region extends substantially from the seventh point to a ninth point of the first drain region located between the seventh and second points, and wherein the portion of the first drain region extending from the ninth point to the second point is at substantially the same horizontal level in the substrate as the first point; and

a second source region with the second dosage formed within the first source region, wherein the second source region extends substantially from the eighth point to a tenth point of the first source region located between the eighth and fourth points, and wherein the portion of

the first source region extending from the tenth point to the fourth point is at substantially the same horizontal level in the substrate as the third point;

wherein a channel region formed in the substrate between the first drain region and the first source region has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region.

25. (Previously Presented) The high-voltage MOS transistor of claim 24 further comprising a field oxide layer substantially abutting the first doped region at the second point.

26. (Previously Presented) A high-voltage MOS transistor comprising:

a first drain region with a first dosage formed in a substrate, wherein the first drain region extends horizontally from a first point proximate to an upper surface of the substrate to a second point proximate to the upper surface;

a gate structure overlying the substrate and covering a portion of the first drain region extending from the first point to a third point of the first drain region located between the first and second points;

a spacer in contact with the gate structure and covering a portion of the first drain region from the third point to a fourth point of the first drain region located between the third and second points;

a second drain region with a second dosage formed within the first drain region, wherein the second drain region extends substantially from the fourth point to a fifth point of the first drain region located between the fourth and second points, and wherein the portion of the first drain region extending from the fifth point to the second point is at substantially the same horizontal level in the substrate as the first point; and

a source region formed in a substrate on the opposite side of the gate structure from the first drain region, wherein a channel region formed in the substrate between the first drain region

and source region has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region,

wherein the first drain region has a doping concentration of approximately 7.0 to 9.0E12 ions/cm^2.

27. (Previously Presented) A high-voltage MOS transistor comprising:

a first drain region with a first dosage formed in a substrate, wherein the first drain region extends horizontally from a first point proximate to an upper surface of the substrate to a second point proximate to the upper surface;

a gate structure overlying the substrate and covering a portion of the first drain region extending from the first point to a third point of the first drain region located between the first and second points;

a spacer in contact with the gate structure and covering a portion of the first drain region from the third point to a fourth point of the first drain region located between the third and second points;

a second drain region with a second dosage formed within the first drain region, wherein the second drain region extends substantially from the fourth point to a fifth point of the first drain region located between the fourth and second points, and wherein the portion of the first drain region extending from the fifth point to the second point is at substantially the same horizontal level in the substrate as the first point; and

a source region formed in a substrate on the opposite side of the gate structure from the first drain region, wherein a channel region formed in the substrate between the first drain region and source region has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region,

wherein the second drain region has a doping concentration of approximately 2.0 to 4.0E15 ions/cm^2.

28. (Previously Presented) A high-voltage MOS transistor comprising:

a first drain region and a first source region formed in a substrate and spaced from each other;

a gate structure overlying the substrate, interposing between the first drain region and the first source region, and covering a first portion of the first drain region and a first portion of the first source region;

a first spacer in contact with the gate structure and covering a second portion of the first drain region adjacent to the first portion of the first drain region;

a second spacer in contact with the gate structure and covering a second portion of the first source region adjacent to the first portion of the first source region;

a second drain region formed within the first drain region, wherein the second drain region extends substantially from the second portion of the first drain region in the direction opposite the gate structure and the first spacer, wherein the portion of the first drain region extending beyond the second drain region is at substantially the same horizontal level in the substrate as the first portion of the first drain region; and

a second source region formed within the first drain region, wherein the second source region extends substantially from the second portion of the first source region in the direction opposite the gate structure and the second spacer, wherein the portion of the first source region extending beyond the second source region is at substantially the same horizontal level in the substrate as the first portion of the first source region, wherein a channel region formed in the substrate between the first drain region and the first source region has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region.

29. (Previously Presented) A high-voltage MOS transistor comprising:

a substrate;

a gate structure overlying the substrate, the gate structure having a first side and a second side opposite to the first side;

a first doping region with a first dosage formed in the substrate on the first side of the gate structure and partially covered by the gate structure;

a second doping region with a second dosage formed within the first doping region adjacent to the edge on the first side of the gate structure to serve as a drain region, the second doping region is offset from the first doping region at least by a first gate spacer;

a third doping region with the first dosage formed in the substrate on the second side of the gate structure and partially covered by the gate structure;

a fourth doping region with the second dosage formed within the third doping region adjacent to the edge on the second side of the gate structure to serve as a source region, the fourth doping region is offset from the third doping region at least by a second gate spacer; and

a channel region formed in the substrate between the first and third doping regions by turning on the high-voltage MOS transistor to pass current between the source and drain regions, where a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region.

30. (New) A transistor apparatus, comprising:

a gate structure located over a substrate;

a first doped region located in the substrate on a first side of the gate structure and partially underneath the gate structure, the first doped region formed with a dosage ranging between about 7.0E12 ions/cm^2 and about 9.0E12 ions/cm^2;

a second doped region located in the first doped region adjacent an edge on the first side of the gate structure;

a third doped region located in the substrate adjacent an edge on a second side of the gate structure; and

a channel region located in the substrate between the first and third doped regions and having a resistance per unit length that is substantially equal to a resistance per unit length of the first doped region.

31. (New) The transistor apparatus of claim 30 wherein at least one of the first and second doped regions is a drain region of the transistor apparatus and the third doped region is a source region of the transistor apparatus.

32. (New) The transistor apparatus of claim 30 wherein the gate structure comprises a gate, a gate dielectric layer, and a gate spacer.

33. (New) The transistor apparatus of claim 32 wherein a portion of the perimeter of the first doped region is substantially adjacent a portion of the perimeter of the gate dielectric layer, and wherein a portion of the perimeter of the second doped region is substantially adjacent a portion of the outer perimeter of the gate spacer.

34. (New) The transistor apparatus of claim 30 wherein the first doped region is a phosphorous ion implanted region.

Claims 35 and 36. (Canceled).

37. (New) The transistor apparatus of claim 30 wherein the second doped region and the third doped region are formed with substantially similar dosages.

38. (New) The transistor apparatus of claim 30 wherein at least one of the second and third doped regions is formed with a dosage ranging between about 2.0E15 ions/cm^2 and about 4.0E15 ions/cm^2.

39. (New) The transistor apparatus of claim 30 wherein the second and third doped regions are each formed with a dosage ranging between about 2.0E15 ions/cm^2 and about 4.0E15 ions/cm^2.

40. (New) The transistor apparatus of claim 30 wherein at least one of the second and third doped regions is an arsenic ion implanted region.

41. (New) The transistor apparatus of claim 30 wherein at least one of the second and third doped regions is a germanium ion implantation region.